WHAT IS CLAIMED IS:

1. A method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first power line and a first ground line, the first power line and the first ground line being mutually adjacent, the core ring supplying power to circuits surrounded by the core ring, the method comprising:

laying out at least one metal-oxide-semiconductor (MOS) capacitor unit below the core ring, the MOS capacitor unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, at least part of the insulated gate electrode being disposed above part of the active area;

laying out first contacts connecting the active area to one of the first power line and the first ground line, and;

laying out second contacts connecting the insulated gate electrode to another one of the first power line and the first ground line.

2. The method of claim 1, wherein the active area is disposed only below the first power line, the first contacts connecting the active area to the first power line, the second contacts connecting the insulated gate electrode to the first ground line.

3. The method of claim 1, wherein the active area is disposed only below the first ground line, the first contacts connecting the active area to the first ground line, the second contacts connecting the insulated gate electrode to the first power line.

4. The method of claim 1, further comprising laying out a metal guard ring adjacent to the active area of said at least one MOS capacitor unit.

5. The method of claim 1, further comprising:

routing a plurality of the metal interconnecting lines across the core ring, for use as input-output (I/O) signal lines;

identifying a part of the core ring crossed by comparatively few of the I/O signal lines; and

placing said at least one MOS capacitor unit below said part of the core ring.

6. The method of claim 1, further comprising:

calculating an antenna ratio of the first power line; and

calculating an antenna ratio of the first ground line;

wherein laying out said second contacts includes

connecting the insulated gate electrode to the first power line if the antenna ratio of the first power line is greater than the antenna ratio of the first ground line; and

connecting the insulated gate electrode to the first ground line if the antenna ratio of the first ground line is greater than the antenna ratio of the first power line.

7. The method of claim 1, wherein the core ring is surrounded by an I/O ring for supplying power to I/O circuits disposed outside the core ring, the I/O ring including a second power line and a second ground line, the method further comprising:

laying out at least one additional MOS capacitor unit beneath the core ring; and

routing a pair of the metal interconnecting lines from said at least one additional MOS capacitor unit to the I/O

ring.

8. The method of claim 1, wherein the core ring is surrounded by an I/O ring for supplying power to I/O circuits disposed outside the core ring, the I/O ring including a second power line and a second ground line, the method further comprising:

laying out at least one additional MOS capacitor unit between the core ring and the I/O ring; and

routing a pair of the metal interconnecting lines from said at least one additional MOS capacitor unit to the I/O ring.

9. A method of laying out an integrated circuit having a semiconductor substrate and metal interconnecting lines disposed above the semiconductor substrate, the metal interconnecting lines including a core ring with a first power line and a first ground line and an input-output (I/O) ring with a second power line and a second ground line, the first power line and the first ground line being mutually adjacent, the second power line and the second ground line being mutually adjacent, the I/O ring and the core ring being mutually adjacent, the I/O ring surrounding the core ring, the core ring supplying power to circuits surrounded by the core ring, the I/O ring supplying power to I/O circuits disposed outside the core ring, the method comprising:

laying out a plurality of MOS units below the core ring and the I/O ring, each MOS unit having an active area disposed in the semiconductor substrate and an insulated gate electrode disposed on the semiconductor substrate, the active area underlying the first power line, the first ground line, the second power line, and the second ground line, the insulated gate electrode paralleling the active

area and having a plurality of branches overlying the active area; and

laying out contacts connecting the MOS units to the core ring and the I/O ring, the contacts causing at least a first one of the MOS units to function as a MOS capacitor connected to the core ring, and at least a second one of the MOS units to function as a protection transistor connected to both the core ring and the I/O ring.

10. The method of claim 9, wherein the contacts connect the active area of the first one of the MOS units to one of the first power line and the first ground line, and connect the insulated gate electrode of the first one of the MOS units to another one of the first power line and the first ground line.

11. The method of claim 9, wherein the contacts connect the active area of the second one of the MOS units to one of the first power line and the first ground line, and also connect the active area of the second one of the MOS units to one of the second power line and the second ground line.

12. The method of claim 11, wherein the contacts also connect the insulated gate electrode of the second one of the MOS units to one of the first ground line and the second ground line.

13. The method of claim 9, further comprising:

routing a plurality of the metal interconnecting lines from the circuits surrounded by the core ring to the I/O circuits, for use as I/O signal lines;

identifying a part of the core ring crossed by comparatively few of the I/O signal lines; and

placing said plurality of MOS units under said part of

the core ring.

14. The method of claim 9, further comprising:

calculating an antenna ratio of the first power line; and

calculating an antenna ratio of the first ground line;

wherein

if the antenna ratio of the first power line is greater than the antenna ratio of the first ground line, the contacts connect the insulated gate electrode of the first MOS unit to the first power line and connect the active area of the first one of the MOS units to the first ground line; and

if the antenna ratio of the first ground line is greater than the antenna ratio of the first power line, the contacts connect the insulated gate electrode of the first one of the MOS units to the first ground line and connect the active area of the first MOS unit to the first power line.

15. The method of claim 9, wherein the contacts cause at least a third one of the MOS units to function as a MOS capacitor connected to the I/O ring.

16. The method of claim 15, wherein the contacts connect the active area of the third one of the MOS units to one of the second power line and the second ground line, and connect the insulated gate electrode of the third one of the MOS units to another one of the second power line and the second ground line.

17. The method of claim 15, further comprising:

counting a number of simultaneously switched outputs in the I/O circuits;

counting a number of protection transistors already connected to the I/O circuits;

connecting a first number of the MOS units, including the second one of the MOS units, to function as protection transistors; and

connecting a second number of the MOS units, including the third one of the MOS units, to function as MOS capacitors connected to the I/O ring; and

determining the first number and the second number from the number of simultaneously switched outputs in the I/O circuits and the number of protection transistors already connected to the I/O circuits.

18. The method of claim 9, wherein the contacts connect the active area of at least a fourth one of the MOS units to the first power line and the first ground line, the fourth one of the MOS units functioning as a protection transistor.

19. The method of claim 18, wherein the contacts connect the insulated gate electrode of the fourth one of the MOS units to the first ground line.